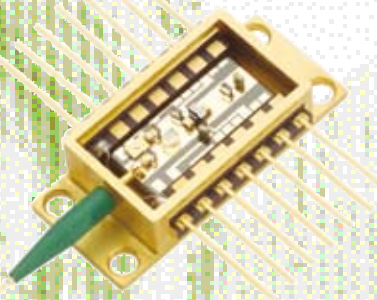
SET Technical Bulletin

DIE BONDING APPLICATIONS



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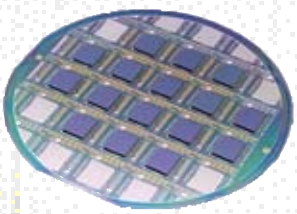

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An Innovative Die to Wafer 3D Integration Scheme: Die to Wafer Oxide or Copper Direct Bonding with Planarised Oxide Inter-Die Filling

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ABSTRACT

An innovative die to wafer stacking is proposed for 3D devices. Known good-dice are bonded on a processed wafer thanks to direct bonding. Oxide layers or patterned oxide/copper layers are used as the bonding medium. After a first thinning, a low stress high deposition rate oxide is deposited to embed the dice. A final thinning is then done to recover a flat and smooth surface before the through silicon vias.

INTRODUCTION

Combining packaging and system on chip technologies, 3D integration is now seen as an alternative solution to the Moore's law. This technique consists in stacking functional components, interconnected by through silicon via (TSV), and thus maintaining or improving the performances of the final circuit at lower manufacturing cost than similar 2D-IC. Direct oxide bonding is a way to address high density TSV integration. Feasibility demonstrations were already achieved at the wafer level using this bonding method (1). While memory stacking is addressed by a wafer to wafer approach, the die to wafer stacking is more suitable for 3D heterogeneous integration, requesting the bonding of various dies sizes coming from different technological nodes or from different substrate material. A die to wafer stack is also the way to answer yield problems by stacking only known good dice. At CEA Leti Minatec, we are implementing an innovative die to wafer 3D integration scheme based on direct bonding and inter-die filling oxide planarisation. The main specification guide line for this new integration is to allow post processes like TSV without any impact on both the direct bonding and the inter-die oxide (meaning no new technology development to be done or any electrical performances degradation of TSV with respect to those obtained on wafer to wafer bonding).

3D INTEGRATION SCHEME

The integration scheme is the following: on a processed wafer, known good dies are bonded by face to face direct bonding in a pick and place tool either with silicon oxide layers or patterned Cu/SiO_2. The dice are then thinned to the wanted thickness. A low stress high deposition rate oxide is deposited all over the structure as an inter-die filling. This oxide is thinned down to the die backside to recover a flat surface before the whole via process is done. Each step of this scheme will be detailed in the following sections. The advantages of this technology are first that direct bonding allows the thinning of the stack down to only a few microns, then since no polymer is used for the bonding or the inter-die filling, thermal strain is reduced and reliability enhanced, finally post processes are not limited by the bonding layers stability with temperature.

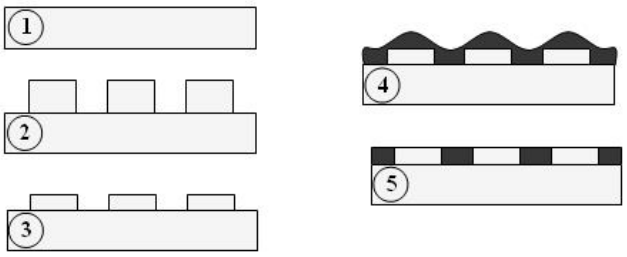

Figure 1 - On a processed wafer (1), known good dies are bonded by direct bonding (2). After a first thinning of the dice (3), a low stress high deposition rate oxide is used as an inter die filling (4). A final planarization is done to allow the via post process (5).

DIE TO WAFER BONDING WITH OXIDE LAYERS

Both die and wafer present continuous surface oxide layer, with buried copper metallization for electrical tests. Surfaces are prepared for direct bonding by mean of mechanical steps (polishing) and chemical steps to achieve high hydrophilic degree. With this preparation a bonding energy G of 1.4 J/m^2 was measured by the double cantilever beam technique on wafer to wafer bonding. Aligned chip-to-Wafer (DtW) structures are realized in an **FC300** equipment from SET to obtain the sub-micrometers alignment required for 3D high interconnection density. Pick&place is then achieved using low pressure (<500mg), at room temperature (~25°C) and for very short contact delay (<20sec). Figure 2 shows an optical microscopy observation of 25 dies bonded on a processed wafer after such a pick&place bonding and a 400°C annealing. After the 400°C annealing, a few non bonded areas are observed. Such defects are attributed to particle contamination of the wafer that occurs during the pick&place sequences. DtW alignment was controlled using Infra-Red microscopy. A misalignment below 1µm was achieved for all the structures. This indicates that high alignment quality DtW structures could be made using direct bonding and pick&place.

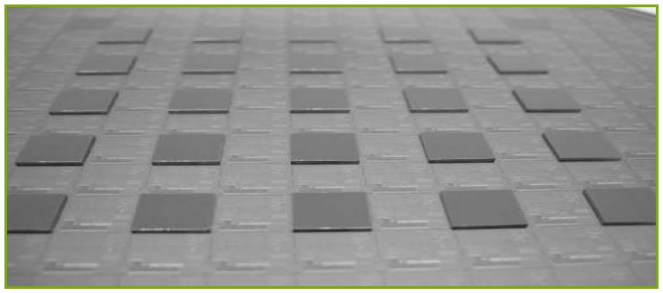

Figure 2 - Optical observation of 25 dies bonded on a processed wafer. The whole structures was annealing at 400°C during 2hrs.

DIE TO WAFER BONDING WITH PATTERNED COPPER/OXIDE LAYERS

Using copper at the bonding interface level is an interesting way to provide both vertical conduction and reliable mechanical toughness (2). To address 3D-ICs applications, an ambient air, atmospheric pressure, room temperature Cu/SiO_2 patterned direct bonding technology has been implemented at the die to wafer level. Low surface roughness, free contamination and flat pattern profile engineering are mandatory to enable high bonding quality (2).

Prior to the dicing, dies are prepared by a CMP process at wafer level to monitor surface adequacy with pattern direct bonding. Since dicing induces huge particle contamination, a die cleaning process is mandatory before bonding. Die to wafer alignment and bonding are then carried out in a SET FC 150 tool. Bonding quality is characterized by Scanning Acoustic Microscopy (SAM) after 200°C/30minutes annealing step. Few non bonded areas are recorded at the patterned bonding interface induced again by particle contamination (Fig. 2). The bonding was effective with copper density of 20% (pad structure and 2% (Kelvin structure). Anyway one as to note that depending of the copper density the bonding energy will range at 200°C from 1.4 J/m² to undebondable structures.

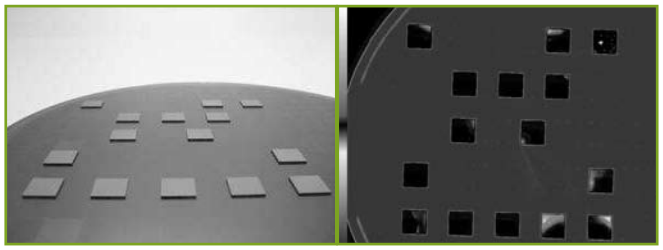

Figure 2 a et b - (left) Optical view of die to wafer SiO_2/Cu patterned direct bonding, (right) Scanning Acoustic Microscopy of the same structure.

The alignment was measured on each die, thanks to cross in box, and ranges from few microns down to 0.5 µm for the best case. The obtained alignment is limited by the capacity of the equipment with our used conditions. Die to wafer SiO_2/Cu patterned direct bonding has been performed with Kelvin structures to allow fine electrical characterization of the bonding interface (Fig. 3). Kelvin structures are obtained by bonding dies on wafers having both a 10 µm branch of the Kelvin structures. The copper to copper contact area is though 10x10µm². The silicon substrates of the dies are removed down to oxide first mechanically and finally with a TMAH wet etch. The silicon oxide is finally dry etched down to the bonding interface to enable probes to connect copper pads (Fig. 4).

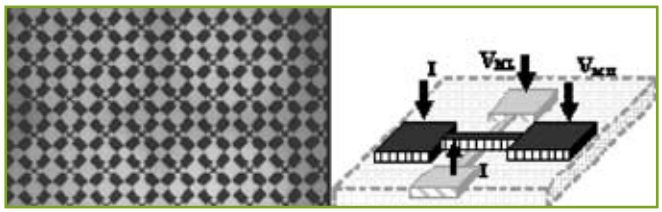

Figure 3 - (left) Infra Red view of Kelvin test structure at the bonding interface before thinning, (right) Principle of the Kelvin structure test.

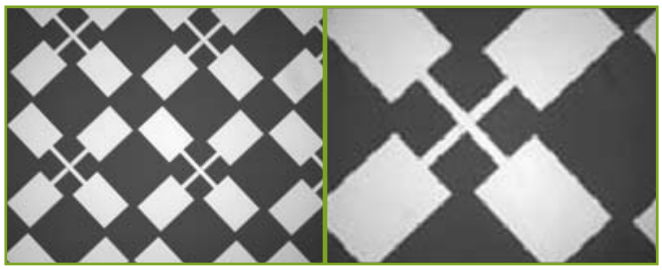

Figure 4 - Optical microscopy of the copper bonding Kelvin structure after silicon and silicon oxide etching. The pads are 95µm large and the bonded zone is 10x10 µm².

Electrical characterization was performed on 400°C/30mn annealed samples. The I(V) curve has a perfect ohmic behaviour (Fig. 5). With four point electrical characterization on Kelvin structures, one can calculate the contact resistance of the copper to copper bonding interface and its specific resistance:

$$R_C = \frac{V_{MH} - V_{ML}}{I}$$

$$\rho_C = R_C \times A_C$$

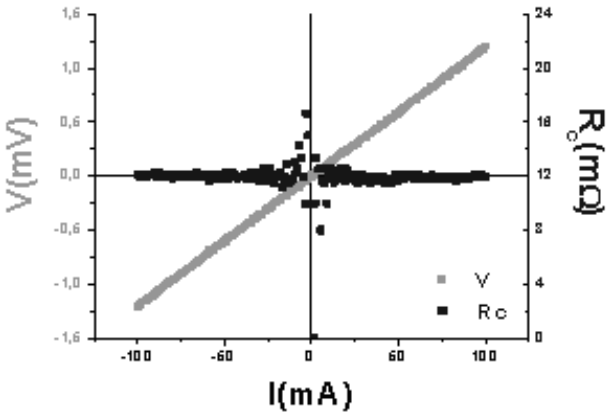

Figure 5 - V(I) and Rc(I) curve on the 10x10 µm² contact area of the Kelvin structure.

With A_c the copper to copper bonded area, V_{MH} the upper

layer electrical potential, V_{ML} the lower layer electrical potential and I the input current. Contact Resistance R_c is 12mΩ for 10x10µm² contact area and the specific contact resistance is 1.2Ω.µm².

This value is in good agreement with wafer to wafer bonding contact resistance measured on similar Kelvin structures (2). Furthermore, this resistance is negligible compare to that of TSV resistance used in 3D IC schemes (1).

INTER DIE FILING AND PLANARISATION

To allow the recovering of a planar surface an inter-die filling must be deposited. For industrial requirements, the filling material must be deposited with an high thickness deposition rate, not be degraded by post process steps (like a 400°C anneal for example), enable an optical alignment through the thick layer and induce a low residual stress. The chosen filling material is a high deposition rate oxide layer with residual low stress. A thickness near 30µm was deposited by PECVD (Plasma Enhanced Chemical Vapor Deposition) at 400°C. Depending on the deposition conditions, the deposition rate ranges from 1.8 to 3µm/mn and the stress in the film as low as 15 MPa.

The stress induced in the dies was simulated with ANSYS software. The stack is described in figure 6, homogeneous anisotropic mechanical properties of interconnects is used.

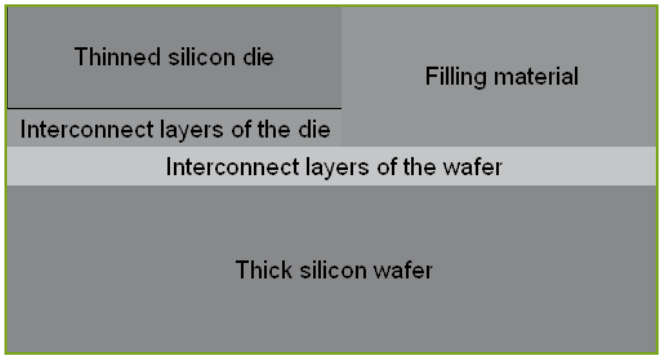

Figure 6 - Simulated area using symmetries of the stack.

Preliminary results show a maximum stress at the edges off the silicon dies of 20 MPa, This stress does not propagate more than a few microns at the edges of the dies.

Figure 7: die to wafer structure after oxide interfiling.

Devices won't be affected by such a stress. Figure 7 is a picture of a wafer after a 30µm thick filling oxide deposition. A recess effect at the edges of the dies appeared after the deposition (Fig. 8). This phenomenon was attributed to a geometric effect and was easily reduced down to 1.4 µm (Fig. 9a).

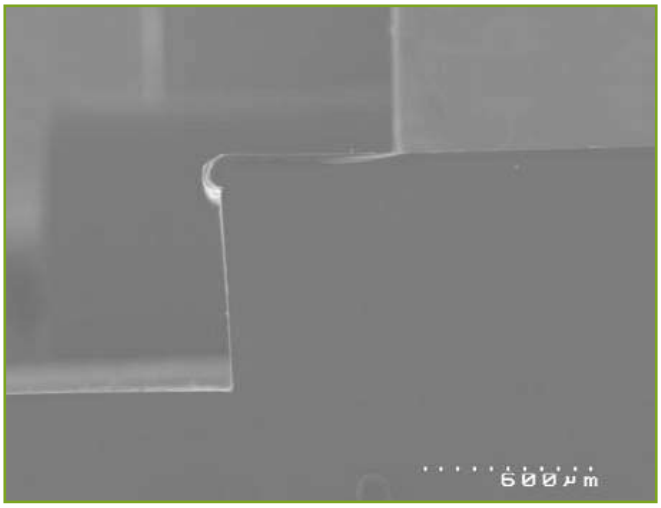

Figure 8 - MEB observation of the oxide deposition on a die, a masking effect is clearly seen at the upper corner of the die.

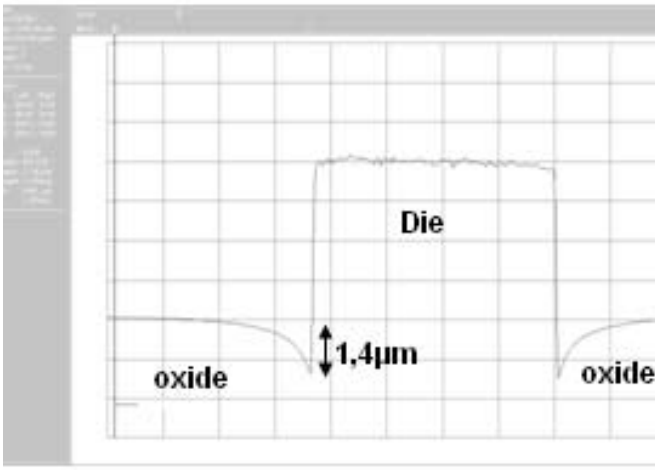

Figure 9a - Oxide recess after deposition measured by profilometry.

In order to recover a flat surface that would allow further technological steps involved in 3D integration processes such as lithography, TSV process or stacking of a second dies level, a planarization stage was developed.

In this process, the oxide layer over the dies is thinned using grinding tools until the recess was removed. Since oxide grinding is very unusual, wheels dedicated to hard material were used. Then, a polishing step is performed to remove the remaining oxide down to the silicon backside, a non selective (Si/SiO_2) specific slurry was used in order to prevent fences creation at the edges of the dies. The targeted final thickness was 15 µm. We obtained a "flat" mixed surface (Si/SiO_2) with a protusion of the silicon dies smaller than 150nm homogeneously on the wafer (figure 9b).

The measured surfaces roughnesses (RMS) are 4nm and 50nm for the silicon and the oxide, respectively. Improvements of this process are still under progress.

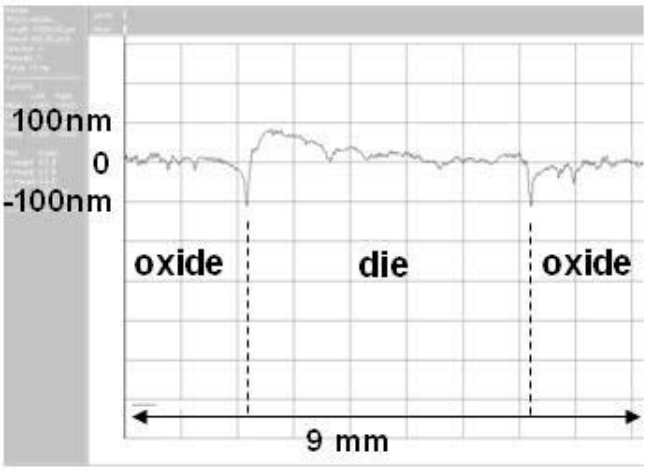

Figure 9b - mechanical profilometer scan of a mixed surface after planrization.

FINAL DEMONSTRATOR

All the described steps were done on processed dies and wafers at a low temperature (< 400°C or < 200°C) to ensure the integrity of the FEOL and BEOL processes already done on the dice or the wafers (Fig. 10). A TSV process described elsewhere (1) was then applied on these wafers without any process adaptation (Fig. 11). The electrical results as for example the measured 3µm TSV resistance of 170mΩ is in good accordance with the values measured for the same structures on bonded wafer to wafer stack. Thus, the feasibility of this innovative 3D integration scheme is demonstrated, improvements are under progress.

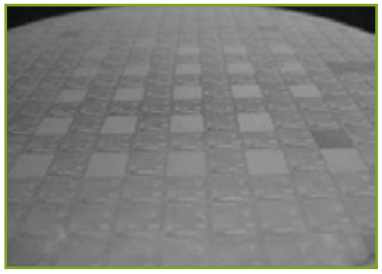

Figure 10: Optical observation of the fully planarised wafer prior to TSV process.

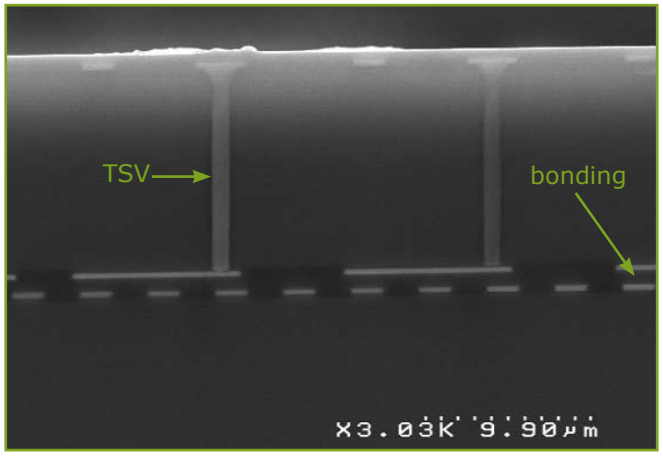

Figure 11 - Cross sectionof the final stack after the TSV process.

CONCLUSION

Each technological step of an innovative 3D die to wafer integration scheme was developed such as: die to wafer bonding with oxide or mixed copper/oxide layer, oxide filling and planarization. and validated in an electrical demonstrator. The obtained results on the first tests are very encouraging. And this technology will be implemented.

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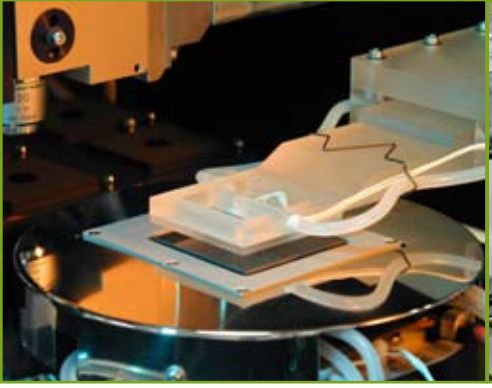

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